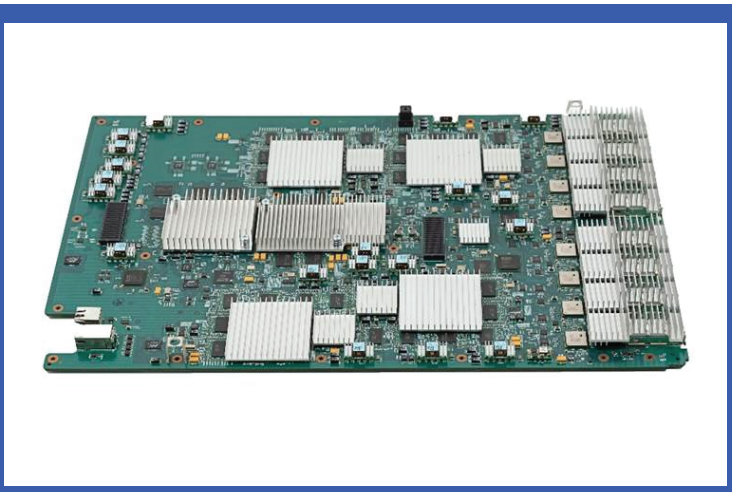
WHiZZ SYSTEMS
Engineering Powered Manufacturing

CASE STUDY

FPGA's Accelerate Hardware Designs



Next generation hardware designs are incorporating the world's fastest silicon with massive gigaflop compute power to drive data throughput. Where these devices were mostly focused on data center and cloud computing, there is now a broad market requirement to deploy FPGA across key markets. Whizz is leveraging their design team to support evaluation and complete turnkey designs to accelerate customer solutions. Their proven services range from early-stage concepts through commercialization and manufacturing.

Market Demand for FPGA's in Hardware Designs

High-performance Field Programmable Gate Arrays (FPGAs) continue to dominate hardware designs in emerging markets where requirements have shifted from flexibility to performance. These complex devices allow for faster time to market than internal proprietary ASIC designs or COTS solutions. The performance of FPGAs has been doubling every 2.5 years and these devices are now being compared with powerful CPUs and GPUs. Xilinx is now considering adding an artificial intelligence engine to their top performing UltraScale+ devices.

The current FPGA's are now being shipped as commercial products into the automotive, 5G infrastructure, data center, gaming, and general embedded systems where there is significant time-to-market demand. Larger, traditional markets such as defense, space, and medical, are also utilizing gate arrays in their commercial designs.

Hardware Design Challenges

There is an ever-increasing demand for hardware design cycles to be compressed in order for the balance of the design including software development, environmental testing, redundancy, and reliability to occur in parallel. Every major market including automotive, aerospace, defense, healthcare, finance, and manufacturing are pouring resources into applications to drive efficiencies, workflows, and services. However, for every new development, there becomes a critical imbalance of staffing resources between hardware and software development. Similar to the expansion of cloud computing, companies are spending more for software talent and this creates a gap for hardware designs.

Addressing the challenges for timing closure, power efficiency, and signal integrity are key to successful designs. Timing closure refers to ensuring that all paths in the design meet the specified timing constraints. FPGAs consist of a vast number of configurable logic elements, interconnects, and other resources. As designs become more complex and clock frequencies increase, it becomes challenging to ensure that signals propagate through the design within the required clock cycles. Meeting timing

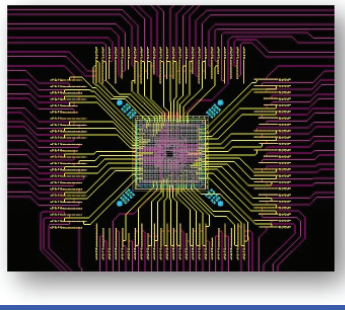
requirements often involves careful placement and routing strategies, using advanced synthesis and optimization tools, and making trade-offs between clock frequency and design performance. High-performance FPGA design is an iterative process that requires expertise in hardware design, FPGA architecture, and a deep understanding of the application domain.

Achieving high-performance in FPGA designs often comes at the cost of increased power consumption. FPGAs can consume significant amounts of power, especially when running at high clock frequencies or when using resource-intensive components like DSP blocks. Balancing the trade-off between performance and power efficiency is a critical challenge. Designers need to implement power-saving techniques such as clock gating, power gating, voltage scaling, and optimizing the usage of resources to minimize power consumption while still meeting performance requirements.

Designing for power efficiency can involve complex considerations, as some power-saving techniques might impact the timing or functionality of the design. Power efficiency is becoming increasingly important due to the emphasis on energy conservation and longer battery life in many applications, including mobile devices, data centers, and edge computing.

Ensuring signal integrity becomes a significant challenge as the data rates and frequencies increase. Signal integrity issues can lead to problems such as reflections, crosstalk, ringing, and jitter, which can degrade the quality of the signals and impact the overall system performance.

Successful mitigation of signal integrity challenges requires collaboration between FPGA designers and board layout engineers, use of specialized design tools and methodologies, and careful consideration of the target application's requirements.



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Leveraging FPGA's to Accelerating Hardware Designs

The performance and reliability of FPGA is surpassing most OEM's ability to create new custom silicon for their designs. Instead, customers are focusing their intellectual property in software applications and markets such as artificial intelligence, deep or machine learning to grow their business. Hardware platforms are migrating to a basic set of high-performance CPU+GPU, and FPGAs.

High-performance FPGA designs require efficient utilization of FPGA resources, including logic cells, memory blocks, DSP slices, and more. As designs become more intricate, managing resource allocation and ensuring scalability can become a challenge. Balancing the trade-offs between using different types of resources and optimizing for the target application's performance can be complex. Oversaturation of specific resources can lead to bottlenecks and reduced performance, while underutilization can result in wasted potential. Additionally, designing for scalability, where a design can be easily adapted to different FPGA sizes or generations, can require careful planning and abstraction.

The team at Whizz Systems has been working with key FPGA providers to develop configurable platforms that are key hardware accelerators. These stand alone platforms range from simple evaluation boards which are ideal for software development to market ready solutions that can be quickly adopted for production. As a complete solutions provider, we offer support across the full design cycle. This includes the initial requirements phase to determine the customer needs for cost-effective boards, to complex high-performance systems. Key elements surrounding the FPGA's will often include microprocessors, customer ASICs, data converter, high-speed memory and power systems. These designs may include blind/buried/micro vias, buried capacitance, precisely controlled impedance, multi-laminate and mixed technology stacks. After hardware design completion, the next effort is to verify mechanical and thermal stability through modeling and simulations. Finally, the system will run through signal and power integrity analysis to improve performance.

Market Readiness & Future Proof Hardware Designs

As solutions become more expensive and complex, there becomes a need to build hardware designs that will extend product life cycles into the future. This will include very high ball count gate arrays, dense pitch grids, and thermal hungry silicon. The requirements for a robust design include expert layout with high layer count printed circuit boards, performance and simulation modeling to insure design integrity. Whizz continues their commitment to a strong engineering design team co-located with state-of-the-art electronics manufacturing capabilities. They have collaborated with commercial FPGA silicon providers for evaluation boards and OEM specific designs.